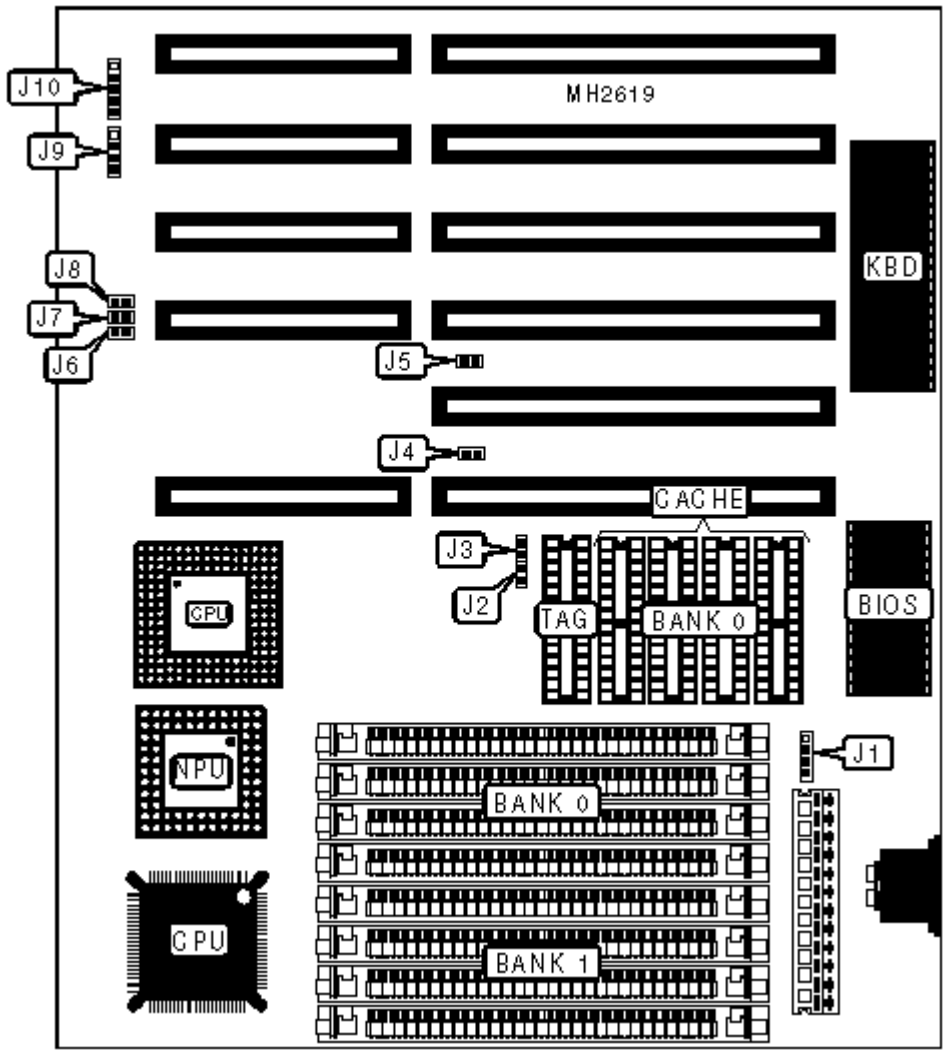
PcChips M326 V5.2

Processor	80386DX/CX486DLC
Processor Speed	33/40MHz
Chip Set	SARC RC4018A4
Max. Onboard DRAM	32MB
Cache	128kB (directly mounted)
BIOS	AMI
Dimensions	220mm x 170mm
I/O Options	None
NPU Options	80387DX



CONNECTIONS			
Purpose	**Location**	**Purpose**	**Location**
External battery	J1	Turbo LED	J8
Reset switch	J6	Speaker	J9
Turbo switch	J7	Power LED & keylock	J10

USER CONFIGURABLE SETTINGS			
Function		**Jumper**	**Position**
»	Cache configuration - do not alter	J2	N/A
»	Cache configuration - do not alter	J3	N/A
»	NPU disabled	J5	Pins 1 & 2 closed
	NPU enabled	J5	Pins 2 & 3 closed

DRAM CONFIGURATION		
Size	**Bank 0**	**Bank 1**
1MB	(4) 256K x 9	NONE
2MB	(4) 256K x 9	(4) 256K x 9
4MB	(4) 1M x 9	NONE
5MB	(4) 256K x 9	(4) 1M x 9

8MB	(4) 1M x 9	(4) 1M x 9
16MB	(4) 4M x 9	NONE
20MB	(4) 1M x 9	(4) 4M x 9
32MB	(4) 4M x 9	(4) 4M x 9

CACHE CONFIGURATION
Note: The cache is soldered on the board without sockets. J2 and J3 are wire jumpers.

CPU SPEED CONFIGURATION	
Speed	**J4**
33MHz	Pins 2 & 3 closed
40MHz	Pins 1 & 2 closed